

## KLT-M3MA-AR1335 PLCC V5.0

On Semiconductor Aptina AR1335\_PLCC MIPI Interface Auto-foco  
13MP Módulo de Câmera



<b>Módulo de câmara No.</b>	<b>KLT-M3MA-AR1335 PLCC V5.0</b>
<b>Sensor de imagem</b>	AR1335_PLCC
<b>EFL</b>	3.81 mm
<b>F.NO</b>	2.2
<b>Pixel</b>	4208 x 3120
<b>Ângulo de visão</b>	74.4°(D) 62.7°(H) 48.7°(V)
<b>Tipo de lente</b>	1/3.2 polegada
<b>Dimensões da lente</b>	8.50 x 8.50 x 5.60 mm
<b>Tamanho do Módulo</b>	19.57 x 8.50 mm
<b>Tipo de Módulo</b>	Auto-foco
<b>Interface</b>	MIPI

**Acasalamento Parte conector No. DF30FC-30DS-0.4V**



Conector de acoplamento na placa principal. Vendido separadamente.

## Product Overview

### AR1335: 13 MP 1/3" CMOS Image Sensor

For complete documentation, see the data sheet.



The AR1335 is a 1/3.2-inch CMOS active-pixel digital image sensor with a pixel array of 4208H x 3120V. The AR1335 digital image sensor, features breakthrough 1.1  $\mu\text{m}$  pixel technology that delivers superior low-light image quality through leading sensitivity, quantum efficiency and linear full well. This allows image quality that rivals digital still cameras. With a sensor architecture focused on low power and a high Chief Ray Angle (CRA) for low Z-heights, the AR1335 is ideal for smartphone and other mobile device applications. It incorporates sophisticated on-chip camera functions such as windowing, mirroring, column and row skip modes, and snapshot mode. It is programmable through a simple two-wire serial interface. The AR1335 sensor can generate full resolution image at up to 30 frames per second (fps) and supports advanced video modes including 4K 30fps, 1080P 60fps and 720P 120fps.

### Features

- 13MP CMOS sensor with advanced 1.1  $\mu\text{m}$  pixel BSI technology
  - Data interfaces: 2,3 and 4 lane MIPI
  - Bit-depth compression available for MIPI: 10-8 and 10-6 to lower bandwidth
  - 3D synchronization controls to enable stereo video capture
  - 6.8 kbits one time programmable memory (OTPM)
  - Programmable controls: gain, horizontal and vertical blanking, auto black level offset correction, frame size/rate, exposure, left-right and top-bottom image reversal, window size, and panning
  - Two on-die phase-locked loop (PLL) oscillators for super low noise performance
  - On-chip temperature sensor
  - Bayer pattern horizontal down-size scaler
  - Simple two-wire fast-mode+ serial interface
- For more features, see the data sheet

### Applications

- Mobile
- 4K video capture
- High resolution still capture

### End Products

- Smart Phone
- Digital Still Camera
- PC Camera
- Consumer devices

### Part Electrical Specifications

Product	Compliance	Status	Type	Megapixels	Frame Rate (fps)	Optical Format	Shutter Type	Pixel Size ( $\mu\text{m}$ )	Output Interface	Color	Package Type
AR1335CSSC11SMD20	Pb-free Halide free	Active	CMOS	13	30	1/3.2 inch	Electronic Rolling	1.1 x 1.1	MIPI	RGB	
AR1335CSSC11SMKA0-CP	Pb-free Halide free	Active	CMOS	13	30	1/3.2 inch	Electronic Rolling	1.1 x 1.1	MIPI	RGB	ODCSP-63
AR1335CSSC11SMKA0-CR	Pb-free Halide free	Active	CMOS	13	30	1/3.2 inch	Electronic Rolling	1.1 x 1.1	MIPI	RGB	ODCSP-63
AR1335CSSC32SMD20	Pb-free Halide free	Active	CMOS	13	30	1/3.2 inch	Electronic Rolling	1.1 x 1.1	MIPI	RGB	
AR1335CSSM11SMD20	Pb-free Halide free	Active	CMOS	13	30	1/3.2 inch	Electronic Rolling	1.1 x 1.1	MIPI	RGB	
AR1335CSSM32SMD20	Pb-free Halide free	Active	CMOS	13	30	1/3.2 inch	Electronic Rolling	1.1 x 1.1	MIPI	RGB	

## Application Diagram



For connectivity above:

- Notes:
- All power supplies should be adequately decoupled; recommended cap values are:
    - 2.7V: 1.0 $\mu$ F and 0.1 $\mu$ F
    - 1.2V: 1.0 $\mu$ F and 0.1 $\mu$ F
    - 1.8V: 1.0 $\mu$ F and 0.1 $\mu$ F
  - Resistor value 1.5k $\Omega$  is recommended, but may be greater for slower two-wire speed.
  - This pull-up resistor is not required if the controller drives a valid logic level on SCLK at all times.
  - VAA and VAA\_PIX must be tied together.
  - Internal charge pump is used for OTPM programming.
  - Digital and MIPI supply can be tied together.
  - ATEST1/AATEST2 must be left floating.
  - TEST pin must be tied to DGND.
  - VDD\_SLVS must be connected to DGND through a bypass cap (0.1 $\mu$ F).

For more information please contact your local sales support at [www.onsemi.com](http://www.onsemi.com).

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